

SEMICONDUCTOR ETCH SPEED MODIFICATION

Zheng, et al

Atty. Docket No. P16463-110578-132742 Express Mail Number EV069127933US, date June 30, 2003

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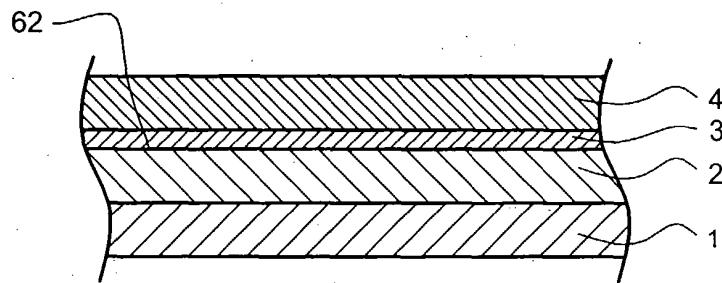


Fig 1

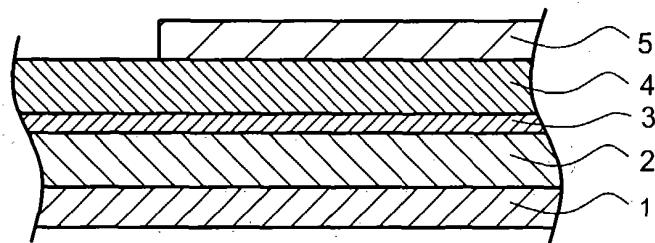


Fig 2

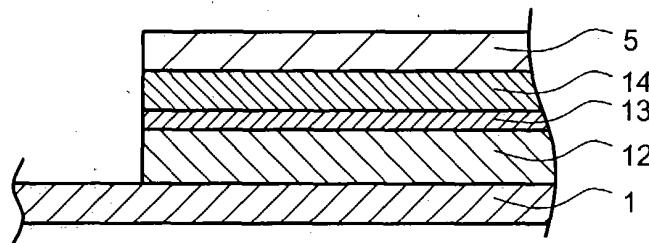


Fig 3

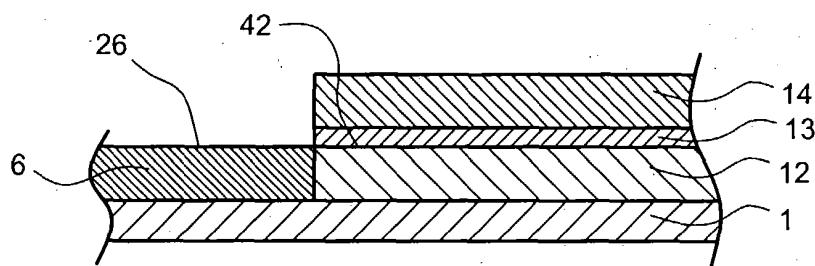


Fig 4

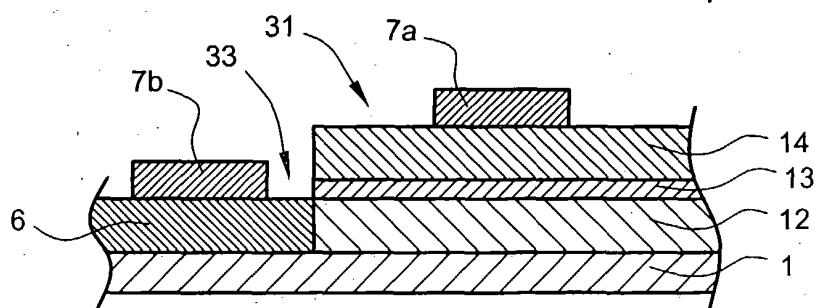


Fig 5

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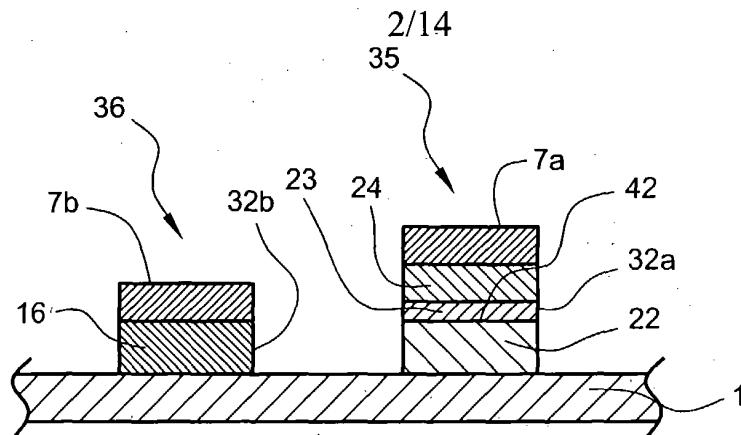


Fig 6A

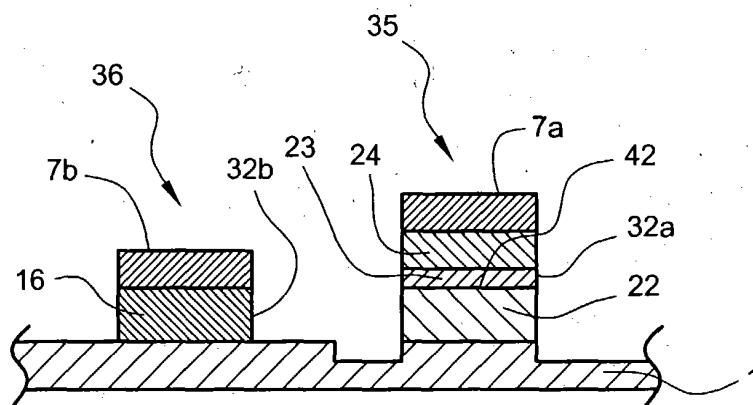


Fig 6B

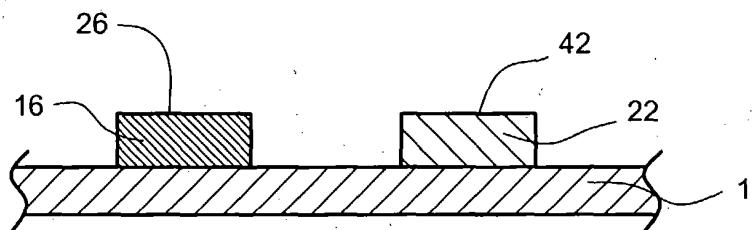
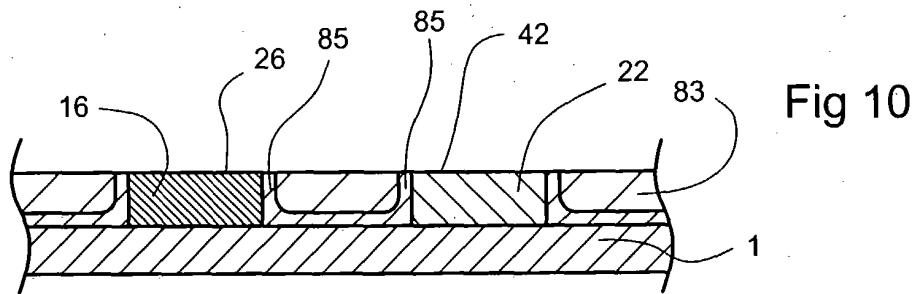
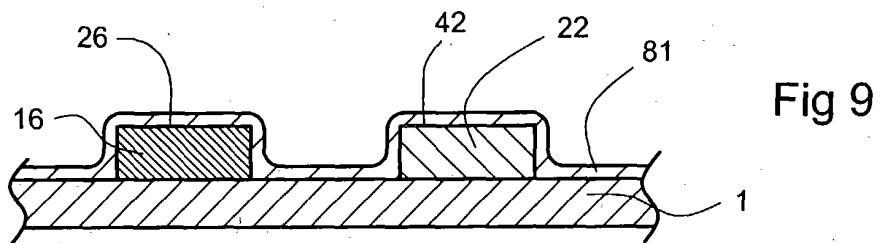
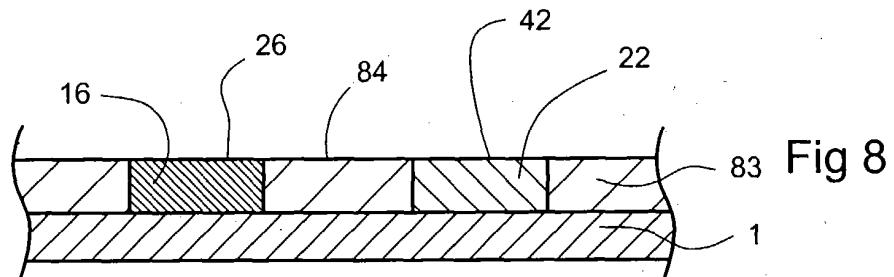
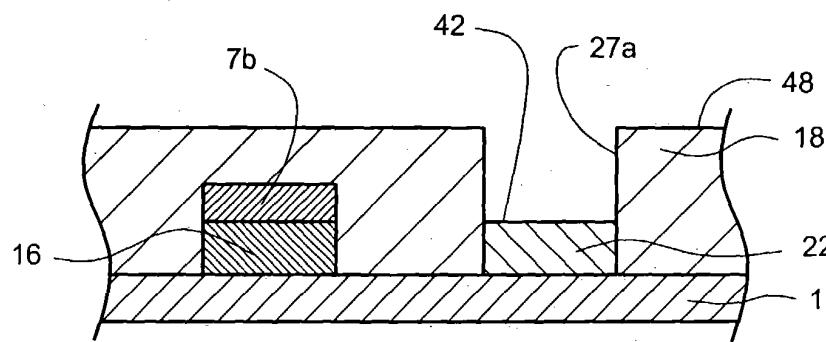
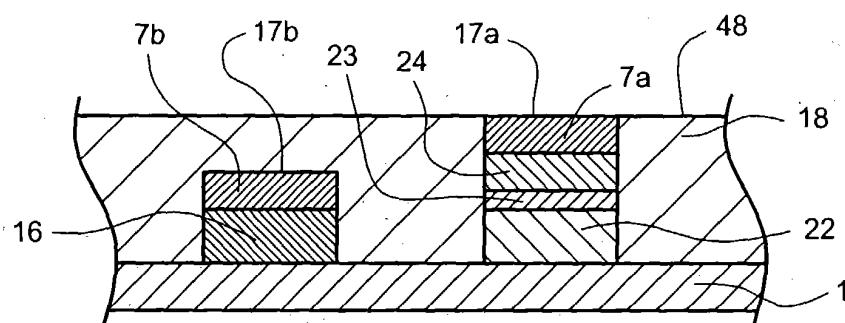
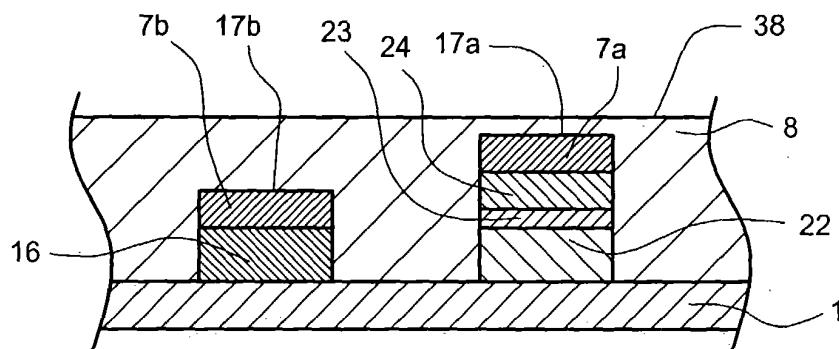


Fig 7

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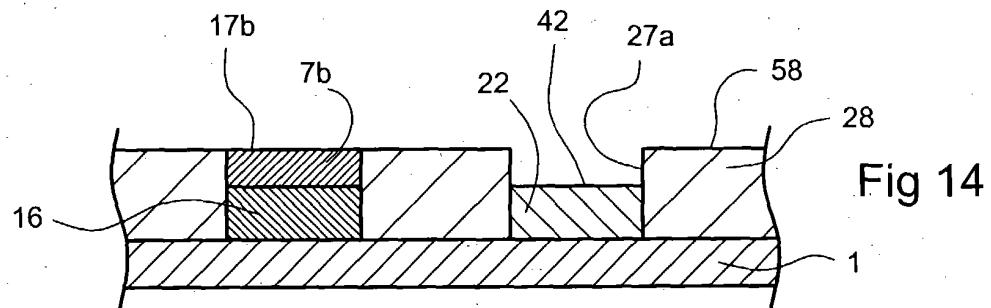


Fig 14

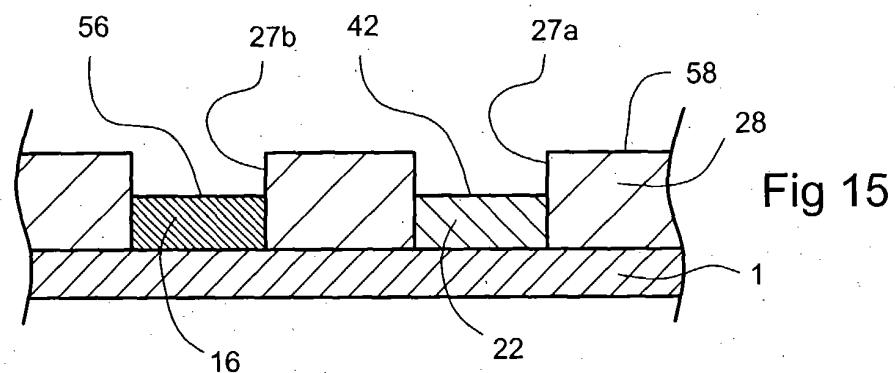


Fig 15

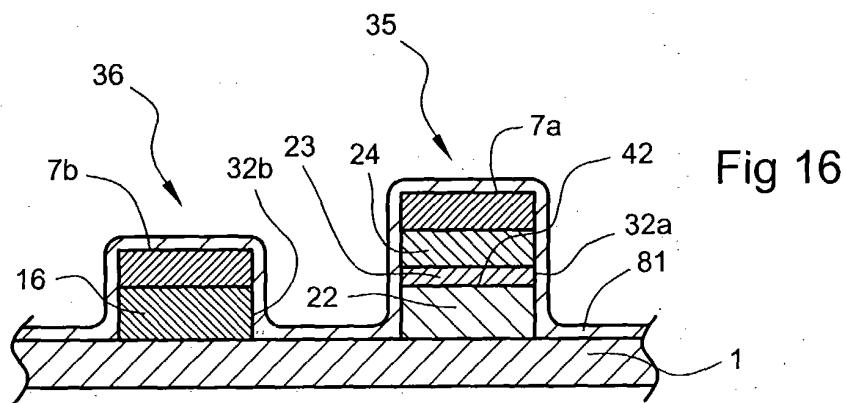


Fig 16

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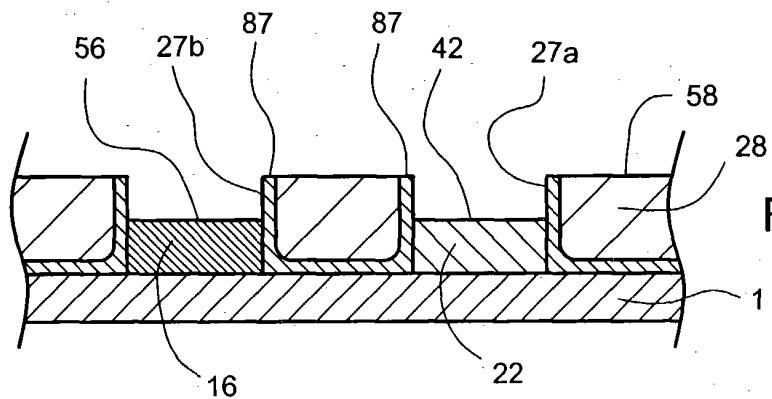


Fig 17

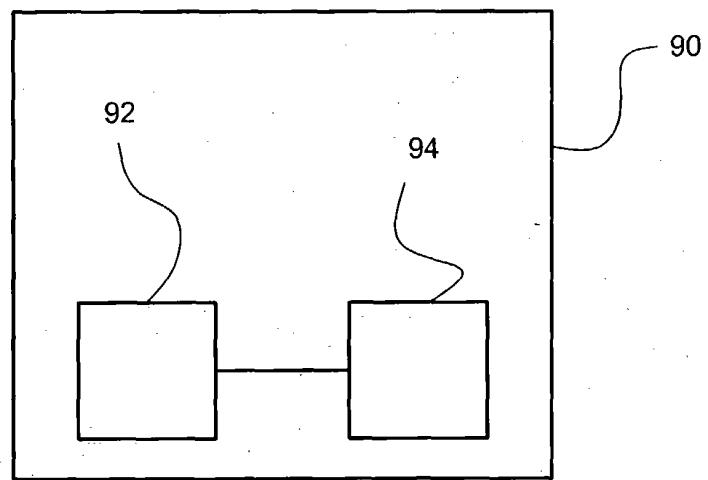


Fig 19

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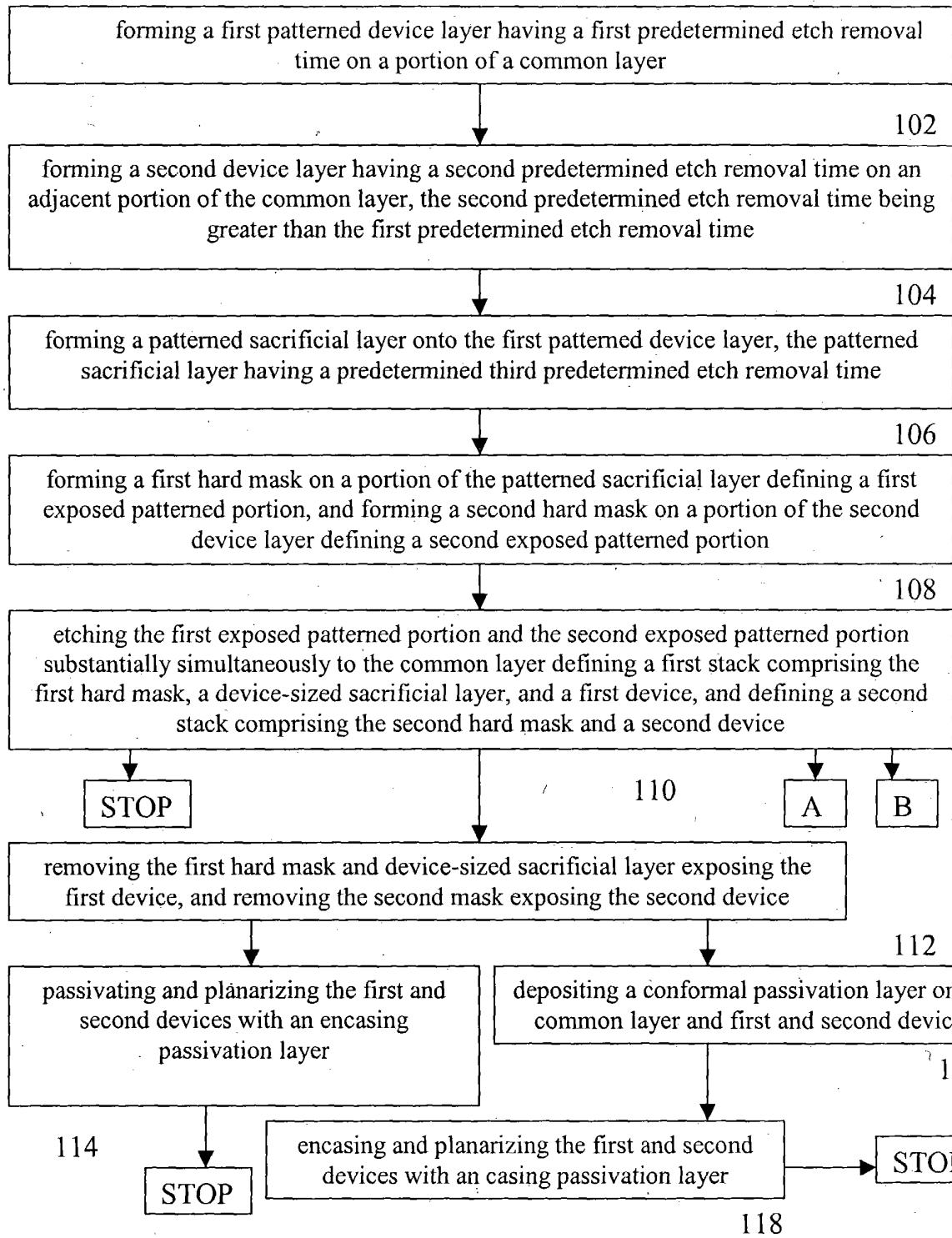


FIG. 18A

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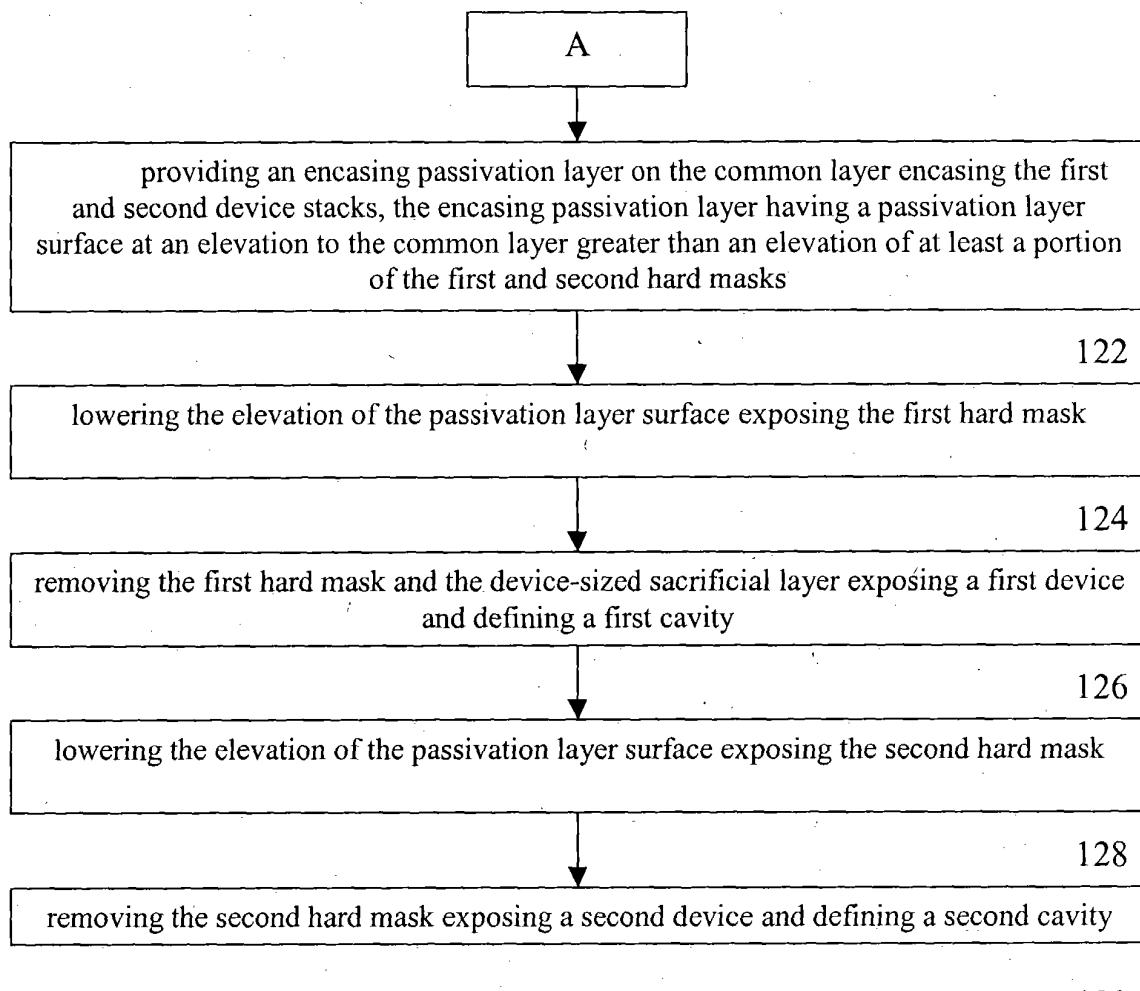


FIG. 18A (continued)

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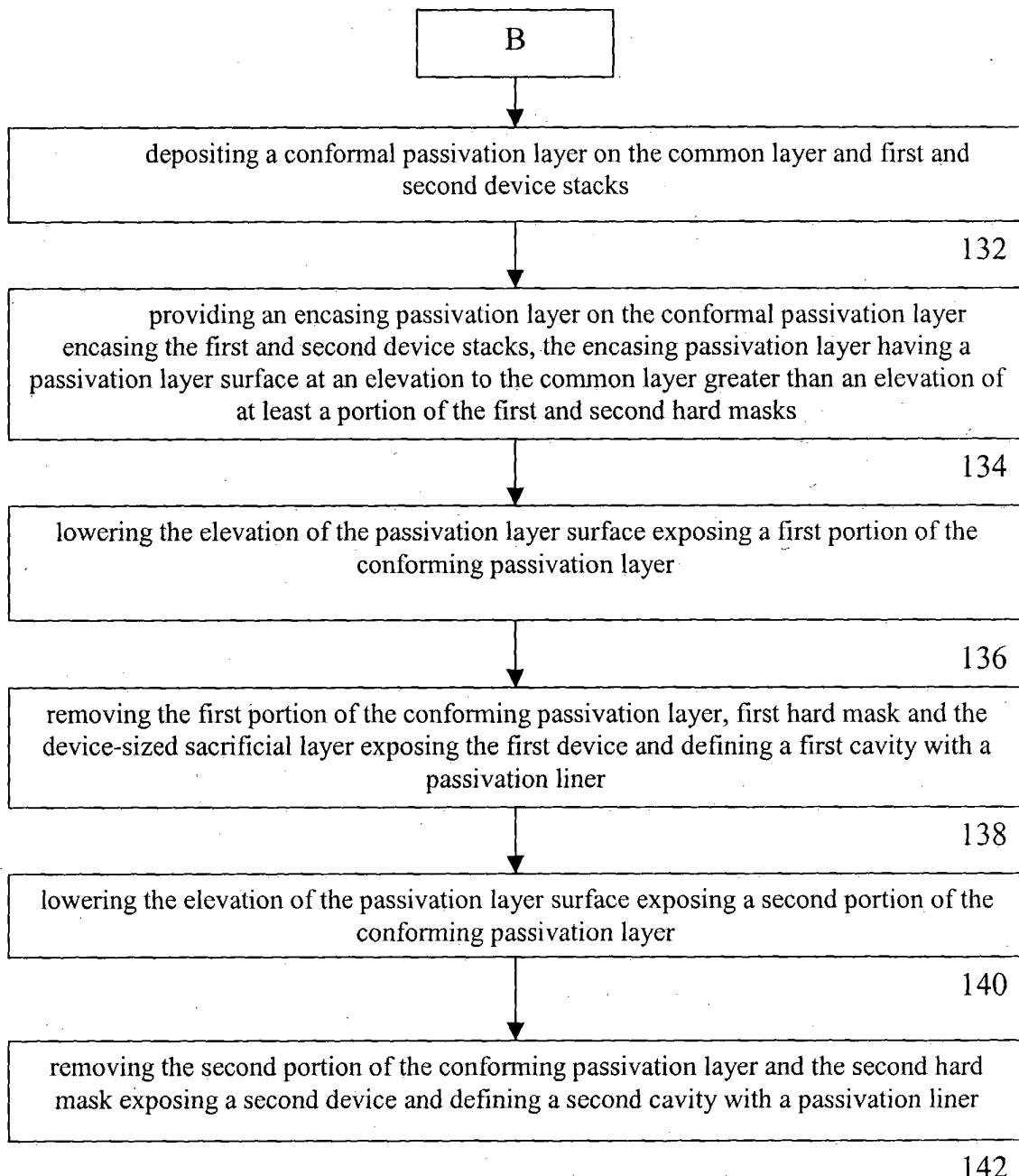


FIG. 18A (continued)

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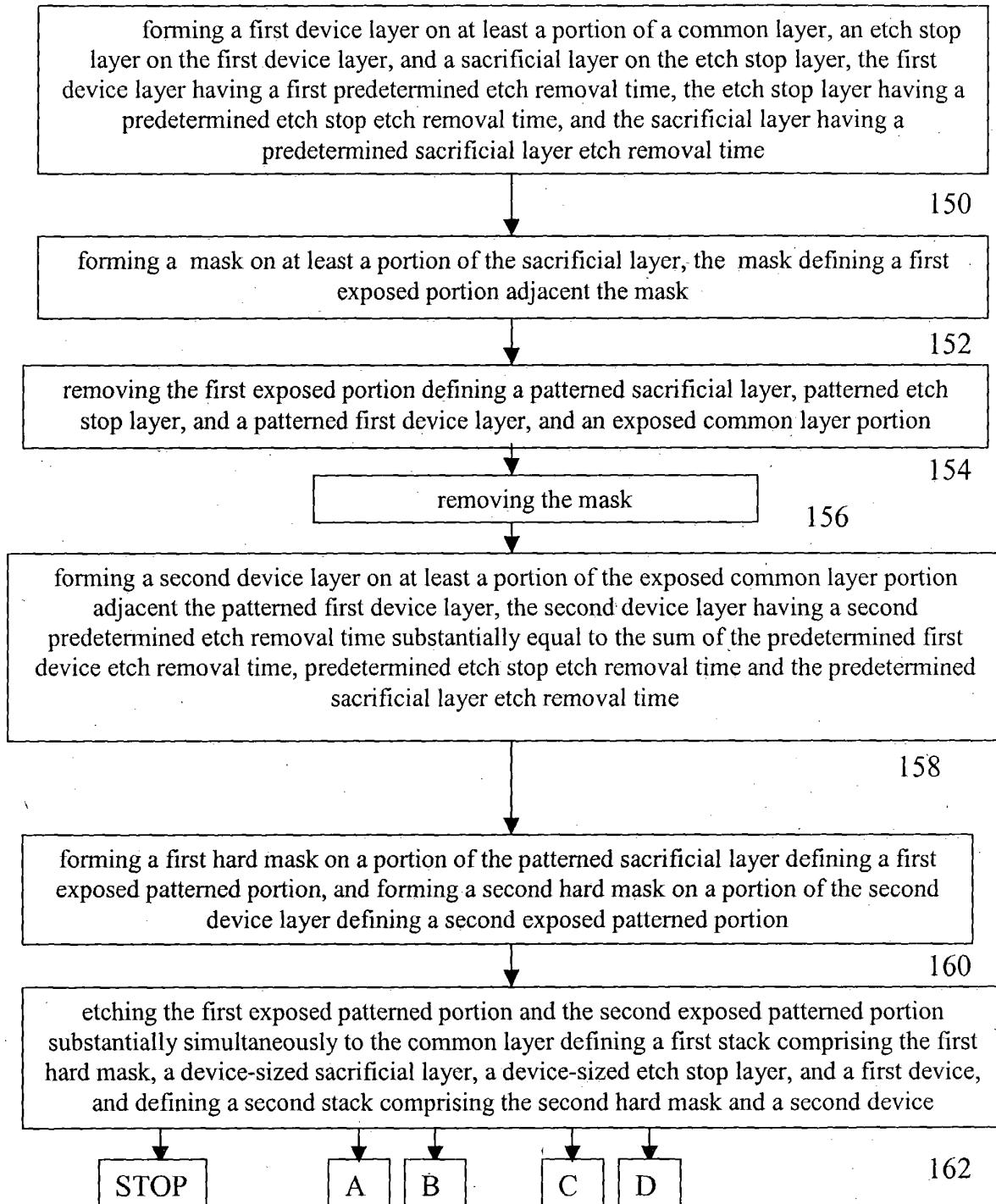


FIG. 18B

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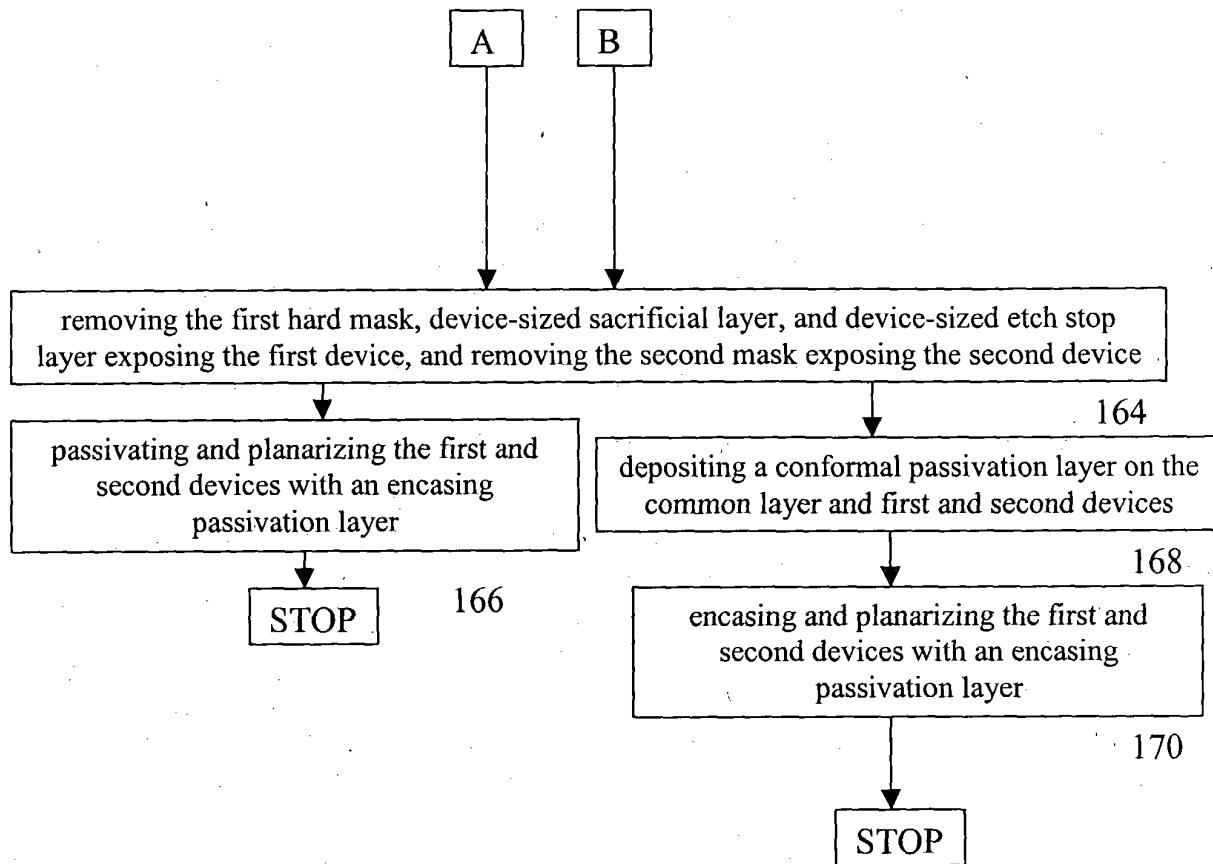
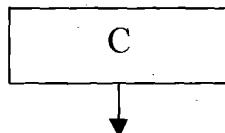


FIG. 18B (continued)

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providing an encasing passivation layer on the common layer encasing the first and second device stacks, the encasing passivation layer having a passivation layer surface at an elevation to the common layer greater than an elevation of at least a portion of the first and second hard masks

172

lowering the elevation of the passivation layer surface exposing the first hard mask

174

removing the first hard mask and the device-sized sacrificial layer exposing a first device and defining a first cavity

176

lowering the elevation of the passivation layer surface exposing the second hard mask

178

removing the second hard mask exposing a second device and defining a second cavity

180

FIG. 18B (continued)

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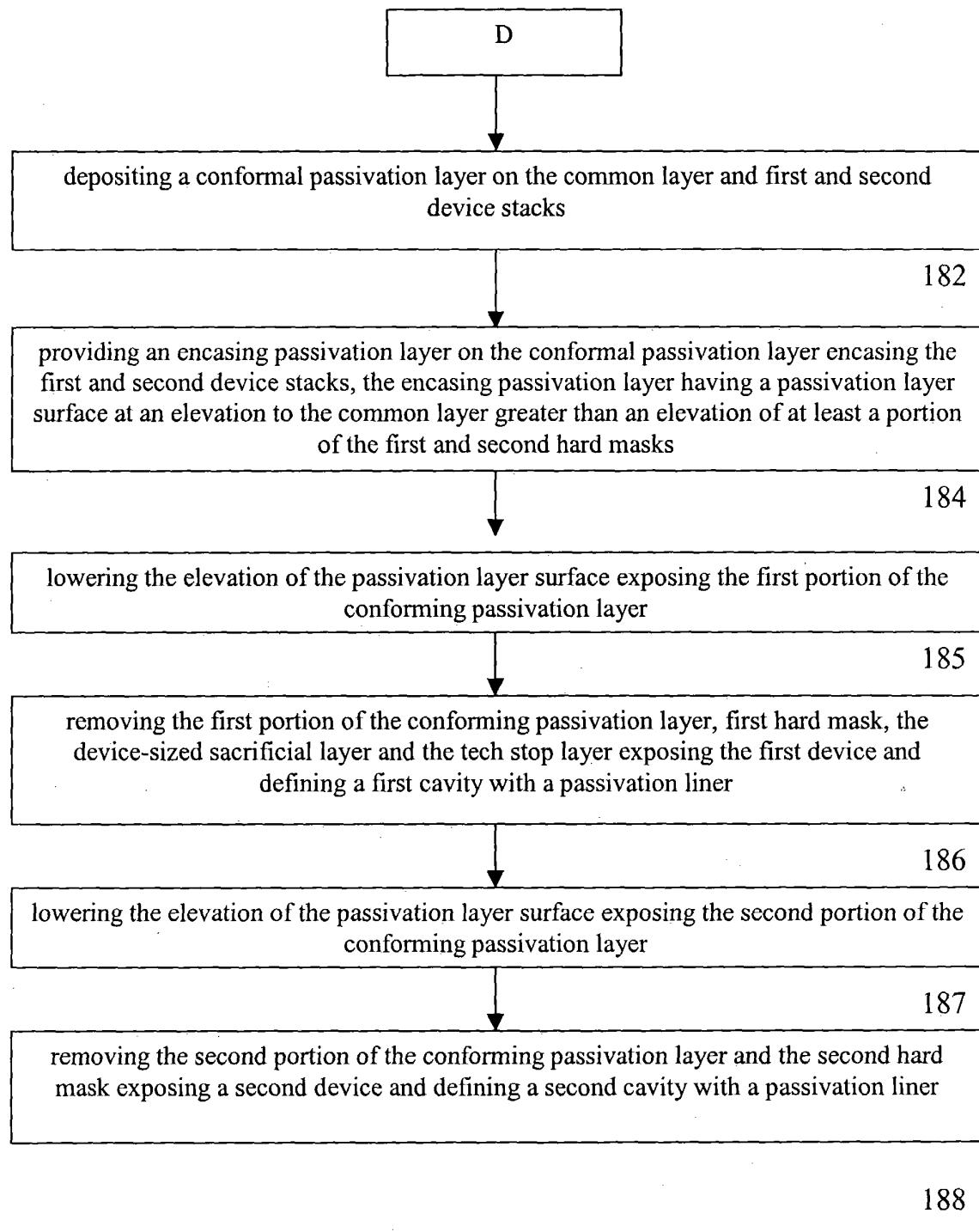


FIG. 18B (continued)

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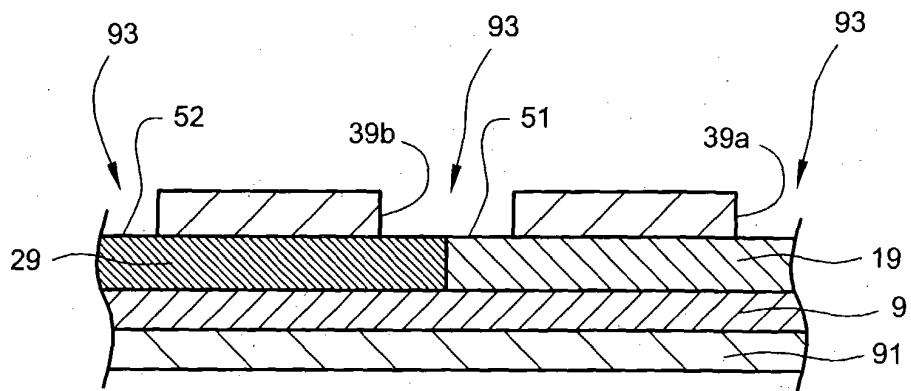


Fig 20A

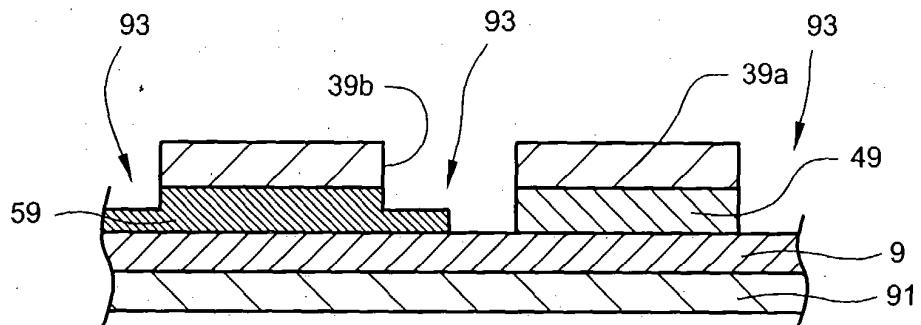


Fig 20B

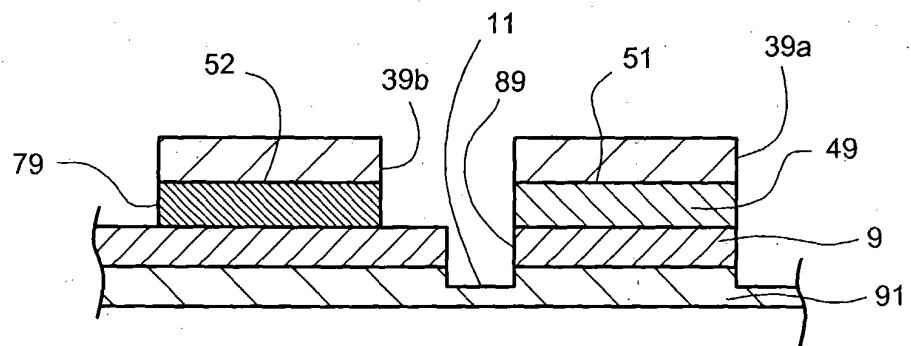


Fig 20C